Claims

1. An optimized bus connection for acceptance of bus transactions, provided with a first store S1 operating according to the FIFO principle, in which transaction processes arriving from a processor system present at a higher level for execution by the optimized bus connection are temporarily stored in the sequence of the arriving transaction processes, characterized in that, following the first store (S1), there is provided a first functional section (I), by which the bus transactions temporarily stored in the first store S1 are read out, classified and typified as fast as possible, in that, following the first functional section, there is provided a second functional section (II) with a plurality of functional lines disposed in parallel, of which at least one is allocated respectively to one class of transactions, in that, by means of the first functional section (I), those transactions that must be executed in a strictly logical sequence are grouped respectively as one class of transactions on the one hand and those transactions that do not have to be executed in a strictly logical sequence are grouped respectively as one class of transactions on the other hand, in that, by means of the first functional section (I), depending on the result of its classification and typification of the transactions, the bus transactions are allocated to one of the functional lines of the second functional section (II), in that the functional line allocated to the class of transactions that must be executed in strictly logical sequence is provided with a storage structure functioning according to the FIFO principle, in that the other functional lines have a storage structure suitable for random accesses, and in that, following the second functional section (II), there is provided a third functional section (III) with an execution unit (AE) common to the functional lines of the

second functional section (II), by means of which the transactions contained in the individual functional lines of the second functional section (II) are organized into a serial sequence for forwarding to the processor system present at a higher level, with the feature that, in given cases, depending on the requirements on the higher-level processor system, transactions from the class of transactions that do not have to be executed in strictly logical sequence are moved ahead of the transactions of the class of transactions that must be executed in strictly logical sequence.

2. An optimized bus connection according to claim 1, characterized in that, for the class of transactions that do not have to be executed in strictly logical sequence, there is provided in the second functional section (II), on the basis of division of transactions into two types, which are read and write transactions, an independent functional line for each.

3. An optimized bus connection according to claim 1 or 2, characterized in that, for bus transactions starting from the bus connection up to the execution unit (AE) of the third functional section (III), there is implemented a shortcut (KW2) which operates on condition that an empty state exists in the first two functional sections (I, II).

4. An optimized bus connection according to one of the preceding claims, characterized in that, for the class of transactions that must be executed in strictly logical sequence, starting from a point of arrival in the second functional section (II) up to the execution unit (AE) of the third functional section (III), there is implemented a shortcut (KW2) which operates on condition that an empty state exists in the functional line allocated to that class.